REMARKS

Applicants appreciate that the Examiner accepted the previous amendments to the drawings.

Claims 1, 7-12, and 22 are pending in the application.

The Examiner rejected claims 1, 7-12, and 22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,428,673 (***Ritzdorf***) in view of Silicon Processing for the VLSI Era, Vol. 1-Process Technology, 2nd ed., Lattice Press: Sunset Beach CA 2000, pp. 799-800 (***Wolf***) and U.S. Patent No. 6,298,470 (***Breiner***). Applicants respectfully traverse this rejection.

Applicants respectfully assert that the combination of ***Ritzdorf***, ***Wolf***, and ***Breiner*** does not disclose, teach, or obviate all of the elements of claims 1, 7-12 and 22 of the present invention. In the Office Action dated May 22, 2003, the Examiner asserted that ***Breiner*** provides elements of averaging the thickness measured in a plurality of points on a semiconductor wafer by citing the "multiple measurements for each data point" and "wafer maps" phrases from ***Breiner.*** Applicants respectfully disagree. These phrases are placed in context by the statement "... wafer data may be collected at any number of points in the fabrication process," in ***Breiner.*** (col. 4, lines 14-15 and lines 60-65). First of all, the "number of points" reference in ***Breiner*** refers to the number of positions in the fabrication process, not the number of points on the semiconductor wafer itself. Additionally, the statement regarding "multiple measurements for each data point" refers to a plurality of measurements of each point of data of interest (*e.g.*, a

point of data of interest may be an electrical test measurement); it does not refer to multiple measurements at different points on a semiconductor wafer, as called for by claims 1 and 22 of the present invention (see col. 4, lines 48-65). For example, this description in ***Breiner*** would not lead one of ordinary skill in the art to understand the term "multiple measurement of each data point" to refer to measuring the thickness at various points on a semiconductor wafer; instead, the phrase would be taken as multiple measurements of the thickness of a given point on the wafer (*i.e.*, a multiple measurements of a data point). Therefore, one of ordinary skill in the art would not obviate the element of averaging thickness measurements from a plurality of points on a semiconductor wafer.

Additionally, the Examiner uses the term "wafer map" to anticipate or at least obviate a wafer map "thickness globally" (see page 4 of the Office Action dated May 22, 2003). Applicants respectfully disagree with this premise. The term "wafer map" as disclosed in ***Breiner*** refers to electrical test characteristics, such as breakdown voltages, leakage currents, resistivity, *etc.*, and using such data to provide a map relating to electrical responses related to the geography of the semiconductor wafer (see col. 4, lines 48-59). There is no disclosure or suggestion to obviate a wafer map relating to the thickness across various portions of the semiconductor wafer. Additionally, *arguendo*, even if a thickness wafer map suggestion were present, there is no disclosure or suggestion in ***Breiner*** to obviate the concept of averaging the thickness measurements from various points on the semiconductor wafer. Furthermore, the term "mean" value referenced by ***Breiner*** refers to the mean value relating to multiple measurements of a data point (see description above), not to multiple thickness values of different points on a semiconductor wafer. As described above, this refers to the mean value for a particular data

point calculated using multiple measurements of that single data point. Therefore, ***Breiner*** does not disclose measuring the thickness of copper layers at a plurality of locations on the copper layer and averaging the resultant data, as called for by the claims of the present invention.

Breiner is directed towards extrapolating known data to a new technology to determine and improve yields. ***Breiner*** discloses using data relating to previous generation IC manufacturing technology and applying them to new generation IC manufacturing technology (see for example, col. 2, lines 54-65, col. 13, lines 44-56). Although ***Breiner*** makes a passing reference to a "mean" value of data points, as described above, ***Breiner*** does not disclose measuring the thickness of copper layers at a plurality of locations on the copper layer and averaging the resultant data, as called for by the claims of the present invention. Therefore, ***Breiner*** does not provide the elements of claims 1 and 22 that are admittedly (by the Examiner) missing from ***Ritzdorf*** and ***Wolf***.

Ritzdorf (even when considered with ***Wolf*** and ***Breiner***) does not teach, disclose, or suggest all of the elements of claims 1, 7-12 and 22. ***Ritzdorf*** is directed towards a system for receiving a wafer for processing, *e.g.*, electrochemical plating. ***Ritzdorf*** discloses forming a seed layer upon a wafer, and transporting the wafer for further analysis or processing (see, for example col. 9, lines 52-55, col. 10, lines 14-16). However, ***Ritzdorf*** does not disclose forming an opening upon a first dielectric layer that is formed above a first structure, upon which a copper layer is formed and controlling a parameter based upon a measured thickness, as called for by claims 1 and 22 of the present invention.

Additionally, ***Ritzdorf***, or any other art cited in the Office Action, does not disclose averaging the thickness data from a plurality of sites on a copper layer, as called for by claims 1 and 22 (both as amended). Controlling a parameter in response to thickness data that is averaged from data relating to a plurality of positions are among the concepts that are not disclosed by ***Ritzdorf***, but are called for by claims 1 and 22 of the present invention. Additionally, adding the disclosure of the damascene process in ***Wolf***, along with the disclosure of ***Breiner***, still would not anticipate all of the elements of claim 1, 7-12 and 22. ***Wolf*** describes depositing metal and dielectric layers (see 2nd paragraph, page 800 of ***Wolf***), but fails to disclose averaging the thickness data from a plurality of sites on a copper layer or modifying a parameter in response to the averaged thickness data, as called for by claims 1 and 22 (both as modified). As described in detail above, ***Breiner*** does not provide the elements of claims 1 and 22 that are missing from ***Ritzdorf*** and ***Wolf***. Therefore, adding the disclosure of ***Wolf*** and ***Breiner*** to the disclosure of ***Ritzdorf*** would not result in all of the elements called for by claims 1 or 22 (both as amended) of the present invention.

Furthermore, based upon at least the arguments provided above, Applicants respectfully disagree with the Examiner that some of the elements called for by claim 1 may be inherent in light of ***Wolf***, ***Breiner***, and ***Ritzdorf***, as the Examiner does not provide evidence to support such an argument. In light of the arguments provided above, all of the elements of claim 1 (as amended) of the present invention are not disclosed, taught, or suggested by ***Ritzdorf***, ***Wolf***, ***Breiner***, or their combination. Thus, claim 1 is allowable. Additionally, for at least the reasons presented above, claim 22 (as amended), which has similar "means" elements relating to the elements of claim 1, claim 22 is also allowed.

Independent claims 1 and 22 are allowable for at least the reasons stated above. Dependent claims 7-12, which depend from independent claim 1, are also now considered to be patentable in light of the above-presented arguments.

Furthermore, ***Breiner*** is focused upon using manufacturing data relating to previous IC manufacturing processes and applying the data to predict yields of new IC technology manufacturing. Wherein, ***Ritzdorf*** is directed towards a system for receiving a wafer for processing, *e.g.,* performing electrochemical plating, forming a seed layer upon a wafer, and transporting the wafer for further analysis or processing, which is different from the teachings of ***Breiner***. Without improper hindsight, one with ordinary skill in the art would not combine ***Breiner*** and ***Ritzdorf*** (along with ***Wolf***) to produce the elements called for by claims of the present invention. However, as described above, even if ***Breiner***, ***Ritzdorf***, and ***Wolf***, were combined, all of the element of claims 1, 7-12 and 22 would not be taught, disclosed, suggested, or obviated by ***Ritzdorf***, ***Breiner***, ***Wolf***, or their combination. Therefore, claims 1, 7-12, and 22 are allowable.

In light of the arguments presented above, Applicants respectfully assert that claims 1, 7-12 and 22 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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